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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DAVID K. VAVRO and JAMES A. MITCHELL

Appeal 2009-008740
Application 09/465,634[1]
Technology Center 2100

Decided: August 27, 2009

Before HOWARD B. BLANKENSHIP, JOHN A. JEFFERY, and DEBRA K. STEPHENS, *Administrative Patent Judges*.

STEPHENS, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134(a) from a non-final rejection[2] of claims 1-4, 6-7, 9-16, and 18-24. We have jurisdiction under 35 U.S.C. § 6(b).

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[1] Although Appellants cite a related Appeal No. 2003-1635 (App. Br. 18 (Related Proceedings App'x)), the issues in that appeal are not germane to the issues before us in the present appeal.

We AFFIRM.

Introduction

According to Appellants, the invention is a system and method related to a digital signal processor that uses independent sub-processors that may be controlled by a master programmable controller (Spec. 32, Abstract).

Exemplary Claim

Claim 1 is exemplary and reproduced below:

1. A digital signal processor comprising:

a programmable, multiply and accumulate mathematical processor;

an input processor that processes input signals to the digital signal processor;

an output processor that processes output signals from the digital signal processor;

a master processor that controls said mathematical processor, said input processor and said output processor provides the timing for the other processors;

a storage to store data from each of said processors so as to be selectively accessible by each of said processors; and

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[2] The Examiner mailed a final rejection on March 7, 2007, but subsequently entered a new ground of rejection and reopened prosecution. *See* Non-final Rej. mailed Dec. 12, 2007, at 2.

wherein each of said processors has a different instruction set than the other processors.

Prior Art

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Balmer	US 5,197,140	Mar. 23, 1993

Rejections

The Examiner rejected claims 1-4, 6, 7, 9-16, and 18-24 under 35 U.S.C. § 103(a) as being unpatentable over Balmer.

GROUPING OF CLAIMS

Appellants argue claims 1-4, 6, 7, 9-16, and 18-24 as a group (App. Br. 10, §(A)). We will, therefore, treat claims 2-4, 6, 7, 9-16, and 18-24 as standing or falling with representative claim 1.

We accept Appellants' grouping of the claims. See 37 C.F.R. § 41.37(c)(1)(vii) ("Notwithstanding any other provision of this paragraph, the failure of appellant to separately argue claims which appellant has grouped together shall constitute a waiver of any argument that the Board must consider the patentability of any grouped claim separately.").

APPELLANTS' CONTENTIONS

Appellants contend the Examiner's last office action concedes that "Balmer has not specifically taught wherein each of said processors has a different instruction set then the other processors", but then suggests that each processor has a different set of required tasks to make the system operate as described (App. Br. 10, §A.). The Appellants argue every computer has a variety of different tasks to perform but that does not equate to a variety of different instruction sets (*id.*). An instruction set is a major architectural component and is either built into the CPU or into microcode and according to Appellants, the different instructions are not an "instruction set" (*id.*). Appellants further argue the Examiner presented a hindsight-reasoning-induced assertion in finding obviousness (*id.*).

EXAMINER'S RESPONSE

The Examiner finds Balmer, in reference to the master processor and the low level/parallel processors (i.e. programmable, multiply and accumulate mathematical processor), states the main reason two different types of processors are necessary is due to the level of processing (Ans. 7, §(10)). The Examiner finds Balmer describes a master processor that uses floating point arithmetic and low level processors that do not (*id.*) The Examiner then finds since Balmer explicitly states that the master processor and the low level processor (i.e. programmable, multiply and accumulate processor) execute different operations, Balmer has explicitly taught that the

master processor and the programmable, multiply and accumulate processor have different instructions sets (Ans. 6-7, §(10)). The Examiner admits Balmer is silent on the specific instruction set of the other processors in the system (e.g. input processor and output processor); however, the Examiner finds since Balmer provides motivation for the master processor and low level processor having different instruction sets - they perform different types of processing and, therefore, require different operations/instruction this motivation applies to the other processors (Ans. 7, §(10)). The Examiner then concludes because these processors perform different types of processing and, therefore, requires different operations/instruction, it would have been obvious for them to have different instruction sets from the other processors in the system (*id.*).

ISSUE

35 U.S.C. § 103(a)

Have Appellants met the burden of showing the Examiner erred in concluding Balmer teaches processors each having a different instruction set?

FINDINGS OF FACT (FF)

Appellants' Invention

(1) The digital signal processor 10 may include a plurality of microprocessors 14, 18, 20, 24, and 26 each having their own instruction

sets (Spec. 3, ll. 16-17). The individual processors need not communicate directly with one another but instead may communicate through storage registers associated with a general purpose 20 register (GPR) 32 that is part of the registers 16 (Spec. 3, ll. 17-20). Thus, the results of an operation performed by one of the processors may be stored in the GPR 32 for access by another processor.

(2) Each of the processors may be separately programmed with its own set of codes (Spec. 3, ll. 23-24). The instruction sets for each processor may provide the logic for operating the particular functions for that processor, avoiding the need for separate hardware logic for implementing the subprocessor functions (Spec. 3, l. 24, to Spec. 4, l. 1).

(3) Although each of the processors may be independently programmed, the instruction sets may be sufficiently similar so that an instruction set for one processor may be modified for use in other processors (Spec. 4, ll. 9-12).

Balmer Reference

(4) Balmer relates generally to an addressing arrangement and method for use in multi-processor systems (col. 1, ll. 6-8).

(5) These processors can be working together in the single instruction, multiple data mode (SIMD) where all of the processors are operating from the same instruction stream but obtaining data from various

sources, or the processors can be working together in the multiple instruction, multiple data mode (MIMD) where each processor is working from a different set of instructions and working on data from different sources (col. 1, ll. 52-60).

(6) In one example, two different types of processors are necessary because of the level of the processing (col. 14, ll. 47-49). The master processor performs high level processing, preferably using floating point arithmetic for high precision, while the low level processors do not require floating point arithmetic and thus can be made faster and smaller (col. 14, ll. 49-60).

(7) The manipulation of these two different types of data representations requires different processing structures which is another motivation for the master and parallel processors having different structures (col. 15, ll. 3-7).

(8) The master processor of the preferred embodiment would have features similar to a RISC processor which is primarily intended for general purpose computing operations, whereas the parallel processors are more like digital signal processors (DSP) which tend to be specialized processors for arithmetic operations (col. 15. ll. 8-13).

PRINCIPLES OF LAW

Claim Construction

"The Patent and Trademark Office (PTO) must consider all claim limitations when determining patentability of an invention over the prior art." *In re Lowry*, 32 F.3d 1579, 1582 (Fed. Cir. 1994) (citing *In re Gulack*, 703 F.2d 1381, 1385 (Fed. Cir. 1983)). "Claims must be read in view of the specification, of which they are a part." *Markman v. Westview Instruments, Inc.,* 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc).

Obviousness

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. *See In re Fine*, 837 F.2d 1071, 1073 (Fed. Cir. 1988). In so doing, the Examiner must make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). Discussing the question of obviousness of claimed subject matter involving a combination of known elements, *KSR Int'l v. Teleflex, Inc.*, 550 U.S. 398 (2007), explains:

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless

> its actual application is beyond his or her skill. *Sakraida* [*v. AG Pro, Inc.*, 425 U.S. 273 (1976)] and *Anderson's-Black Rock*[, *Inc. v. Pavement Salvage Co*., 396 U.S. 57 (1969)] are illustrative—a court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions.

Id. at 417. If the claimed subject matter cannot be fairly characterized as involving the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for the improvement, a holding of obviousness can be based on a showing that "there was an apparent reason to combine the known elements in the fashion claimed." *Id.* at 418. Such a showing requires:

> "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness" . . . . [H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.

Id. (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

If the Examiner's burden is met, the burden then shifts to the Appellants to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. *See In re Oetiker*, 977 F.2d 1443, 1445 (Cir. Fed. 1992).

ANALYSIS

Appellants present a definition of "instruction set."[3] Although the evidence does not provide a copyright date of this reference, we nonetheless find that it was published in 2001. *Id.* As such, we cannot rely on this reference as reflecting what was known in the art to one of ordinary skill in the art at the time the invention was made, namely December 17, 1999. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc) ("[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question *at the time of the invention*, i.e., as of the effective filing date of the patent application.") (emphasis added). Appellants themselves disclose in the Specification that each of the processors may be separately programmed with its instruction set that may provide logic for operating the particular functions for that processor (FF 2). Appellants further disclose the instruction sets of independently programmed processors may be sufficiently similar so an instruction set for one processor may be modified for use in other processors (FF 3).

Balmer teaches different processors that perform different functions (FF 6) and thus, we agree with the Examiner's finding that these processors

[3] "The repertoire of machine language instructions that a computer can follow (from a handful to several hundred). It is a major architectural component and is either built into the CPU or into the microcode. Instructions are generally from one to four bytes long." (Alan Freedman, *Computer Desktop Encyclopedia*, at 470 (9th ed. 2001)).

are executing different instructions. We find the master processor and the low level processors of Balmer use their own set of logic for operating the particular functions for that processor. Additionally, we find Balmer discloses two types of processors – one that is a high precision floating point processor and one which is a faster and smaller low level processor that does not perform floating point arithmetic (FF 6). Therefore, we find the master processor and the low level processors, being of different structures, being of different sizes, and performing different functions, has a different instruction set. We thus find each of the master and low level processors have their own instruction sets.

Since Balmer teaches two processors having their own instruction sets, we conclude one of ordinary skill in the art would have recognized that extending this diversity to each processor such that each had a different instruction set would have been an obvious engineering decision well within the level of skilled artisans. *See KSR*, at 417 ("[I]f a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill."). Appellants have provided no evidence that such a modification would have been beyond the skill of ordinarily skilled artisans.

Accordingly, we conclude that in view of Balmer's teaching of using different processors based on the functions to be performed, it would have

been obvious to one of ordinary skill in the art to use different processors having different instruction sets.

CONCLUSION

Based on the findings of facts and analysis above, we conclude Appellants have not met the burden of showing the Examiner erred in finding Balmer teaches processors each having a different instruction set.

Accordingly, Appellants have not met the burden of showing the Examiner erred in rejecting claims 1-4, 6, 7, 9-16, and 18-24 under 35 U.S.C. § 103(a) for obviousness over Balmer.

DECISION

The Examiner's rejection of claims 1-4, 6, 7, 9-16, and 18-24 under 35 U.S.C. § 103(a) as being unpatentable over Balmer is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

rwk

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